A 700/900mW/Channel CMOS Dual Analog Front-End IC for VDSL with Integrated 11.5/14.5dBm Line Drivers

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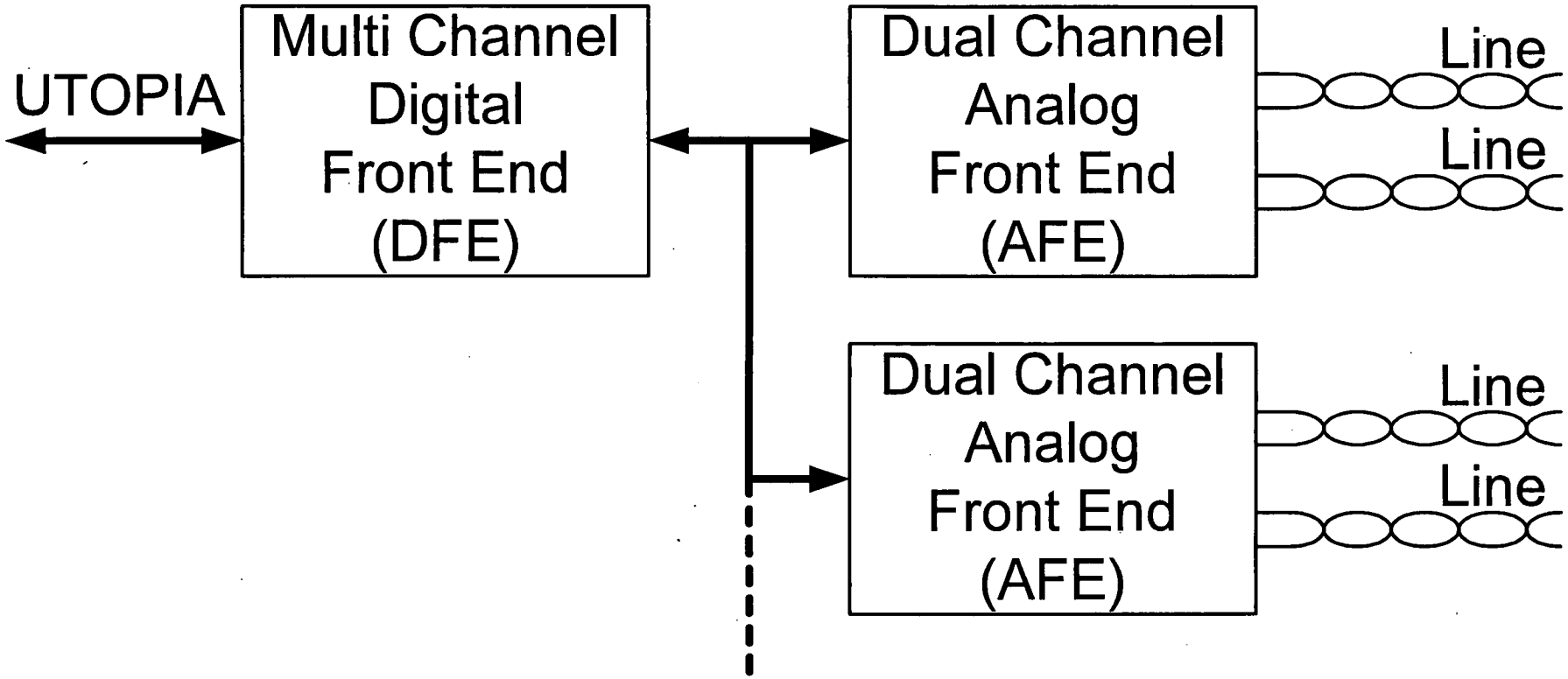
Outline

Dual Channel VDSL AFE

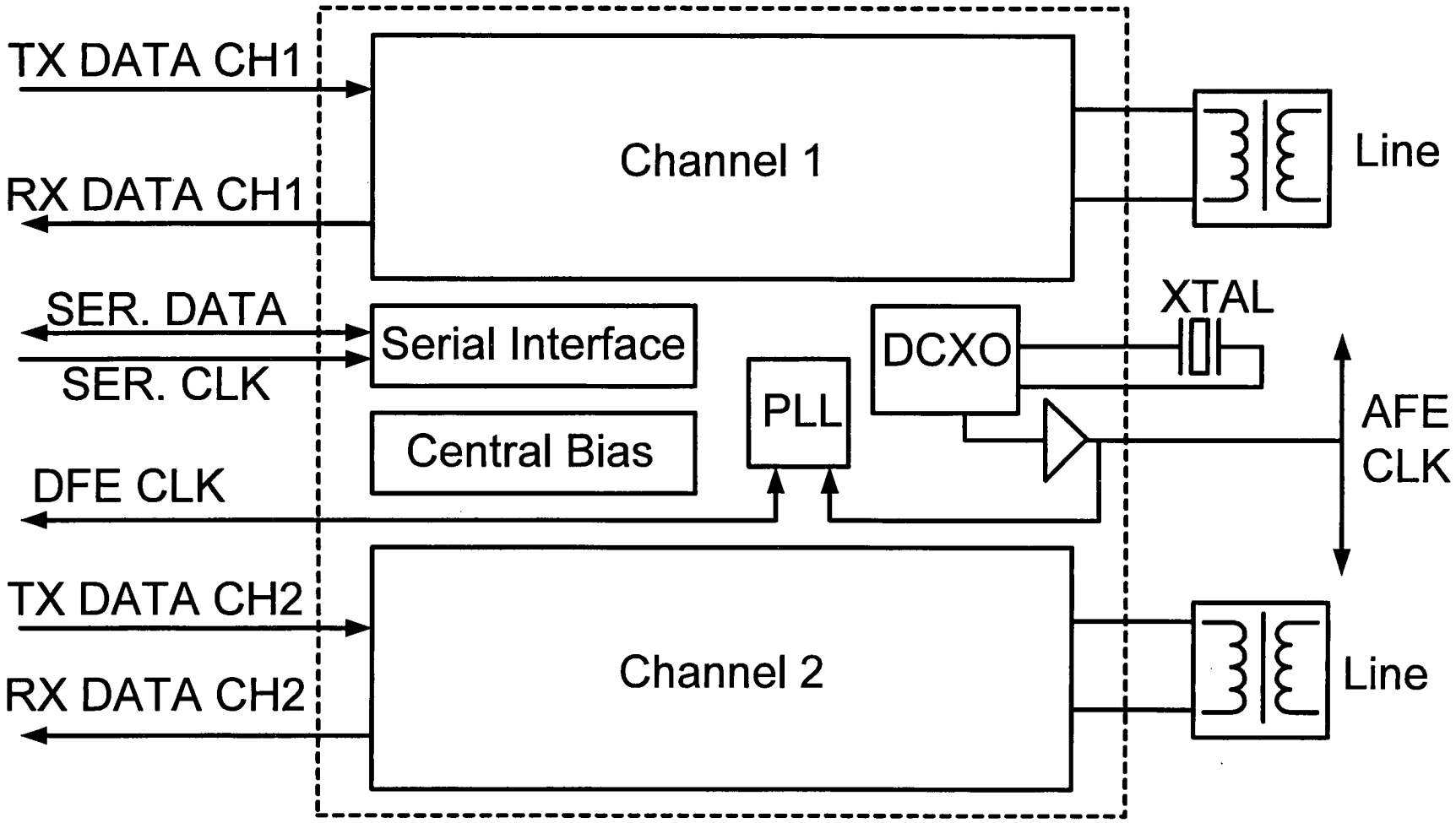
- Overview
- Architecture
- Circuit Implementations
- Measured Performances
- Summary

Overview

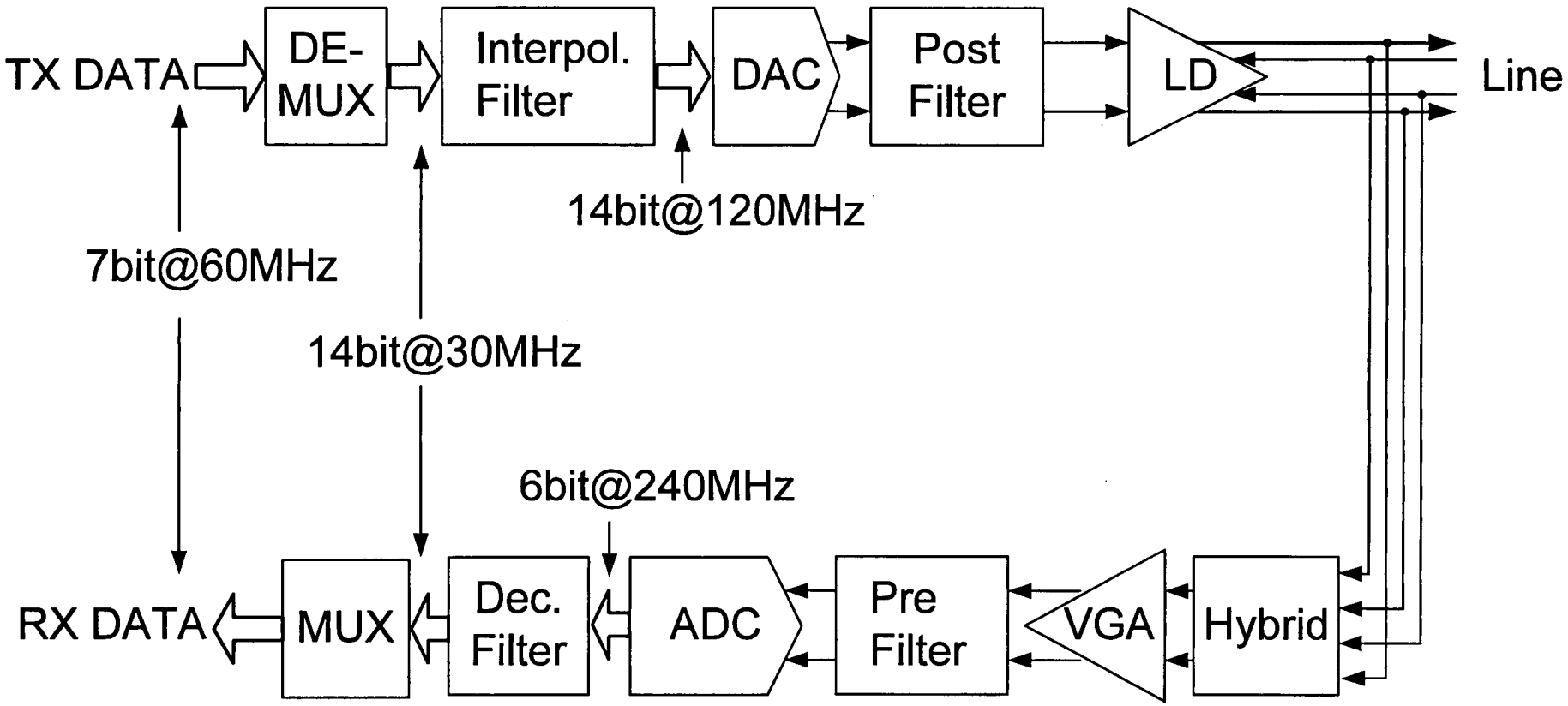


- VDSL-AFE for CO and CPE
- 0.25/0.5μm 5M 1P CMOS, MIM-Capacitors, Poly-Resistors
- Emphasis on power saving
- Almost no external components

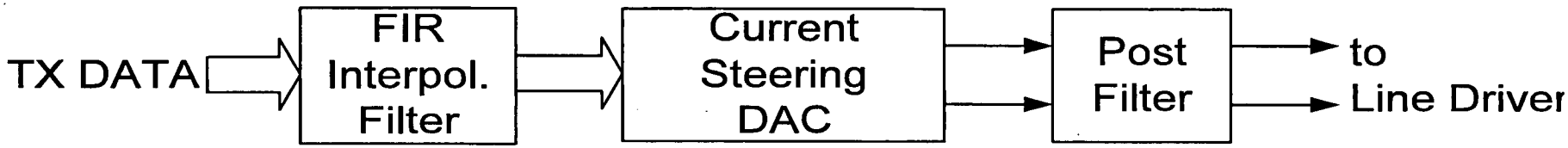
Overview continued

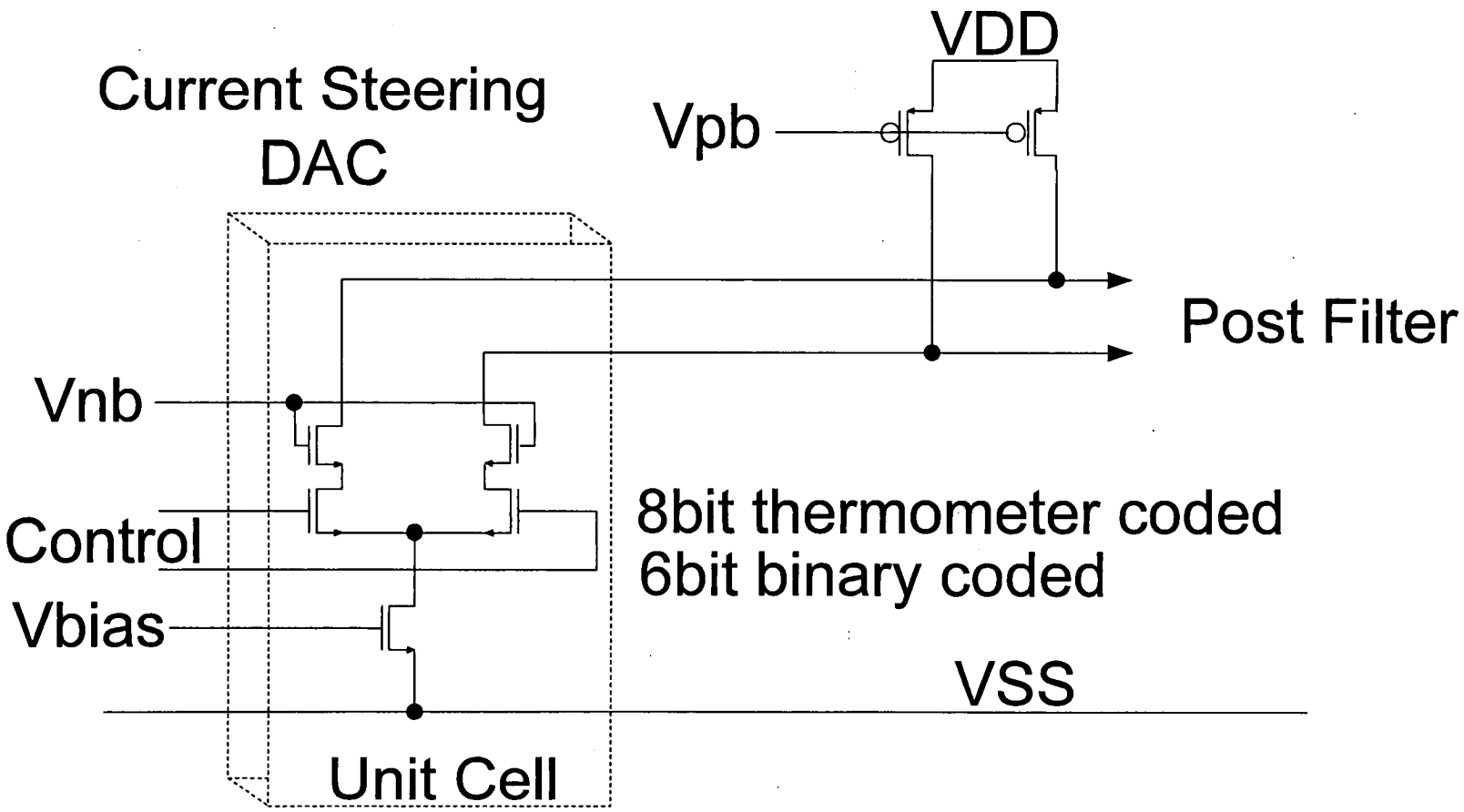


Architecture Per Channel

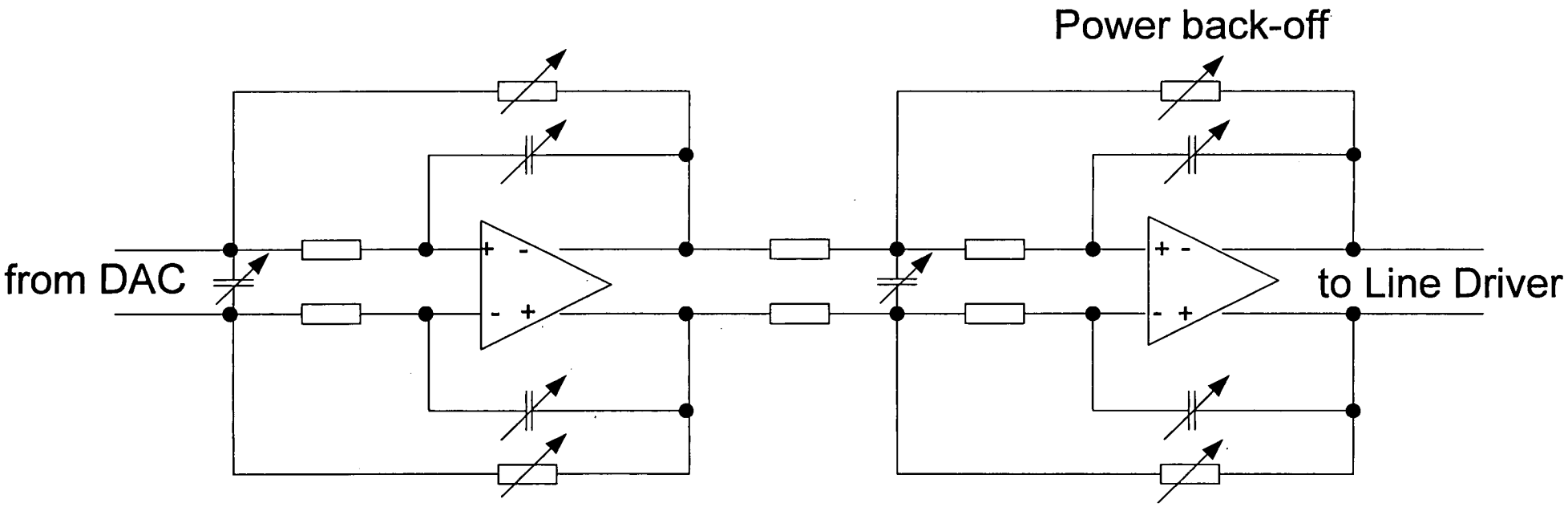


Transmitter Implementation: DAC



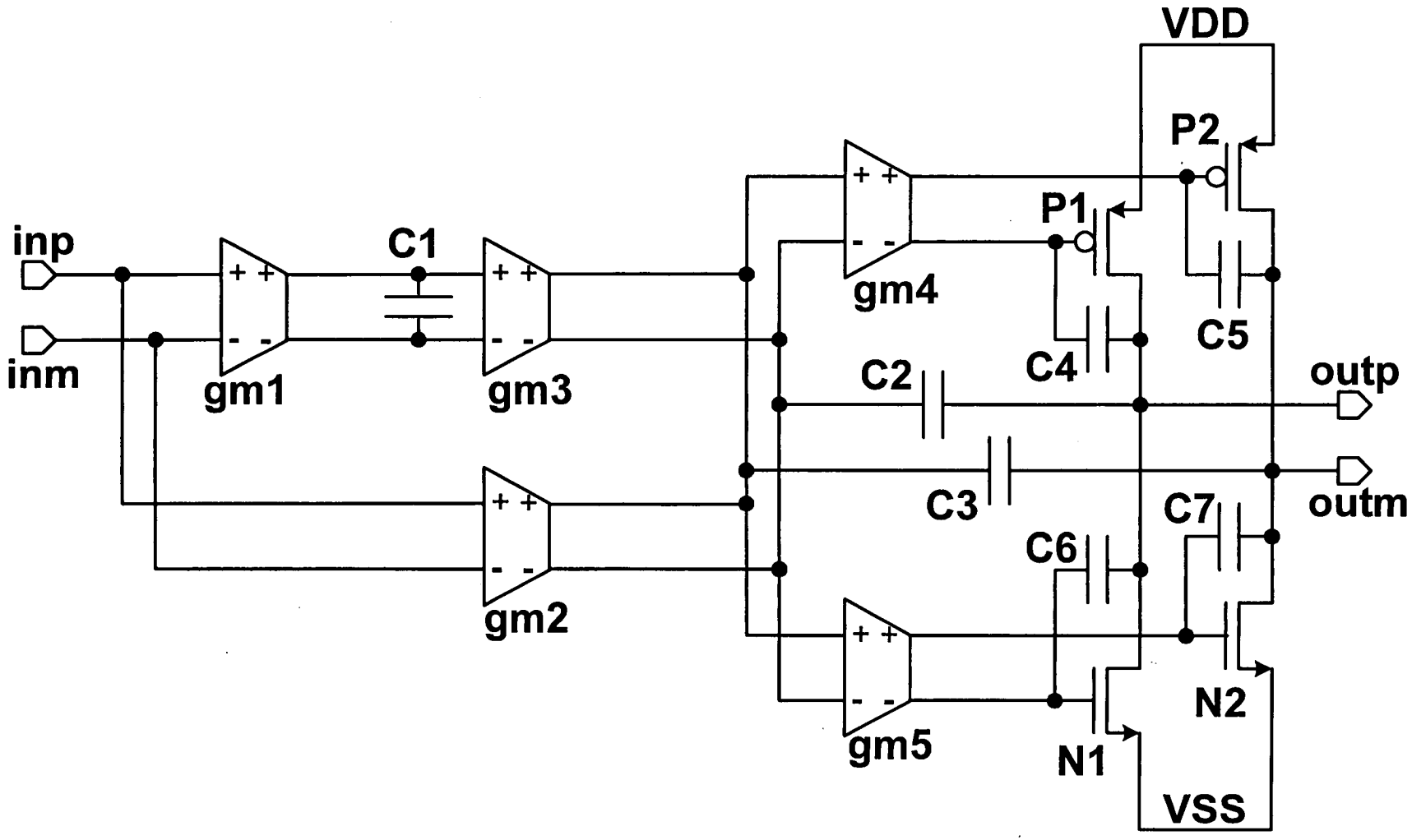


Transmitter: Post Filter

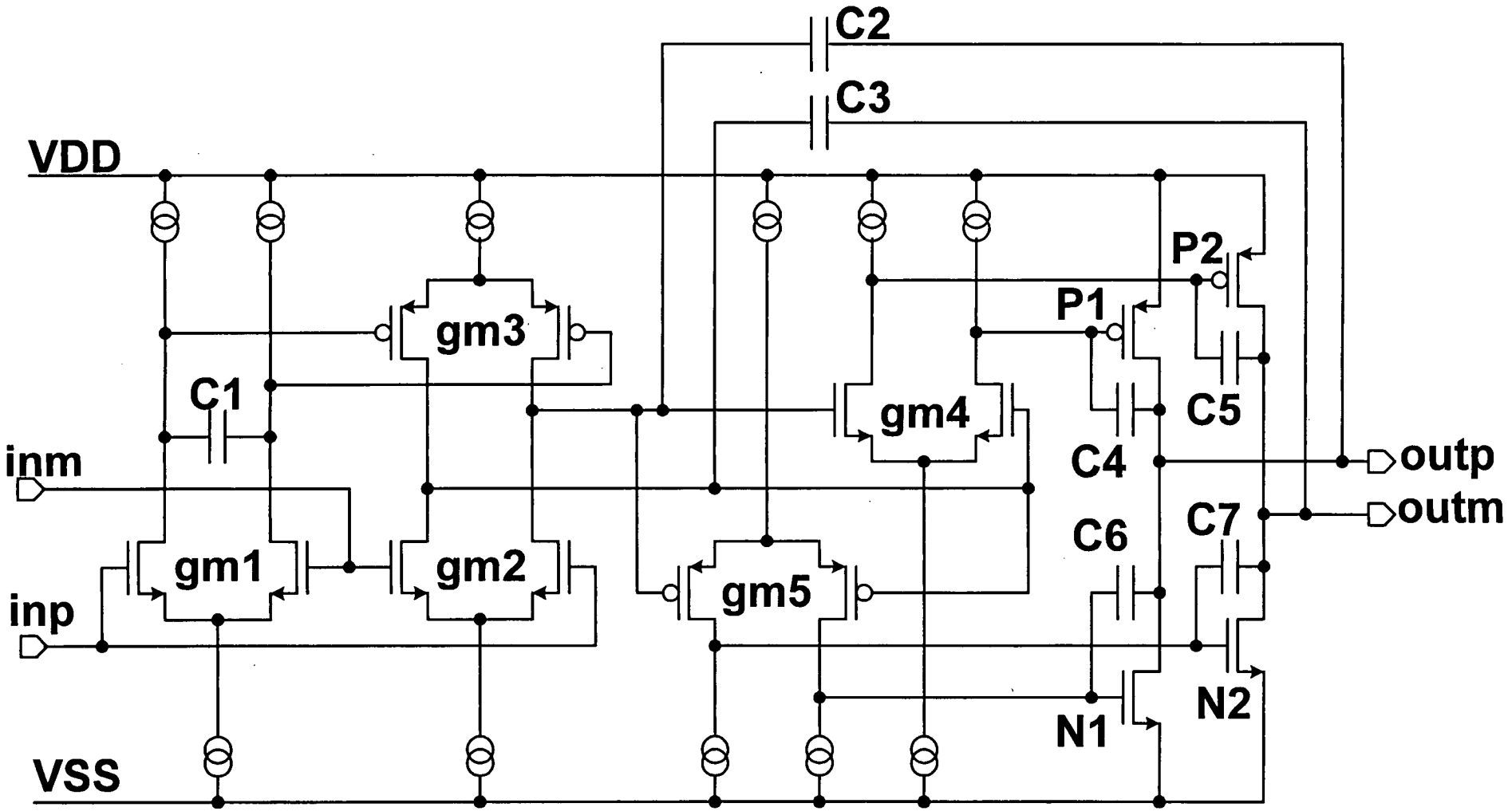


- 4th order Butterworth, f_{-3dB} 18MHz, calibrated at power up
- 14dB Power back-off in 1dB steps

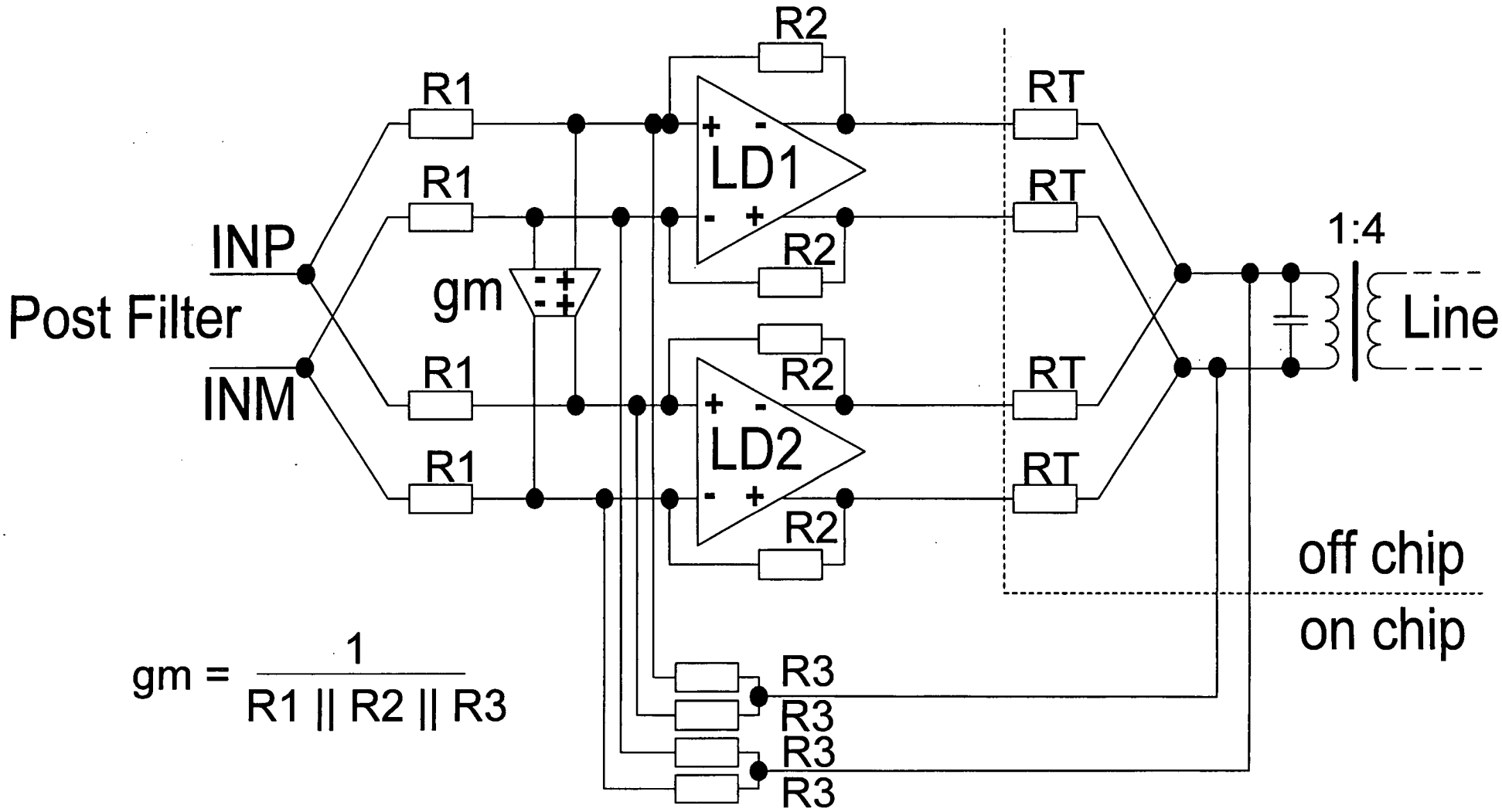
OPAMP CONCEPT



OPAMP CORE

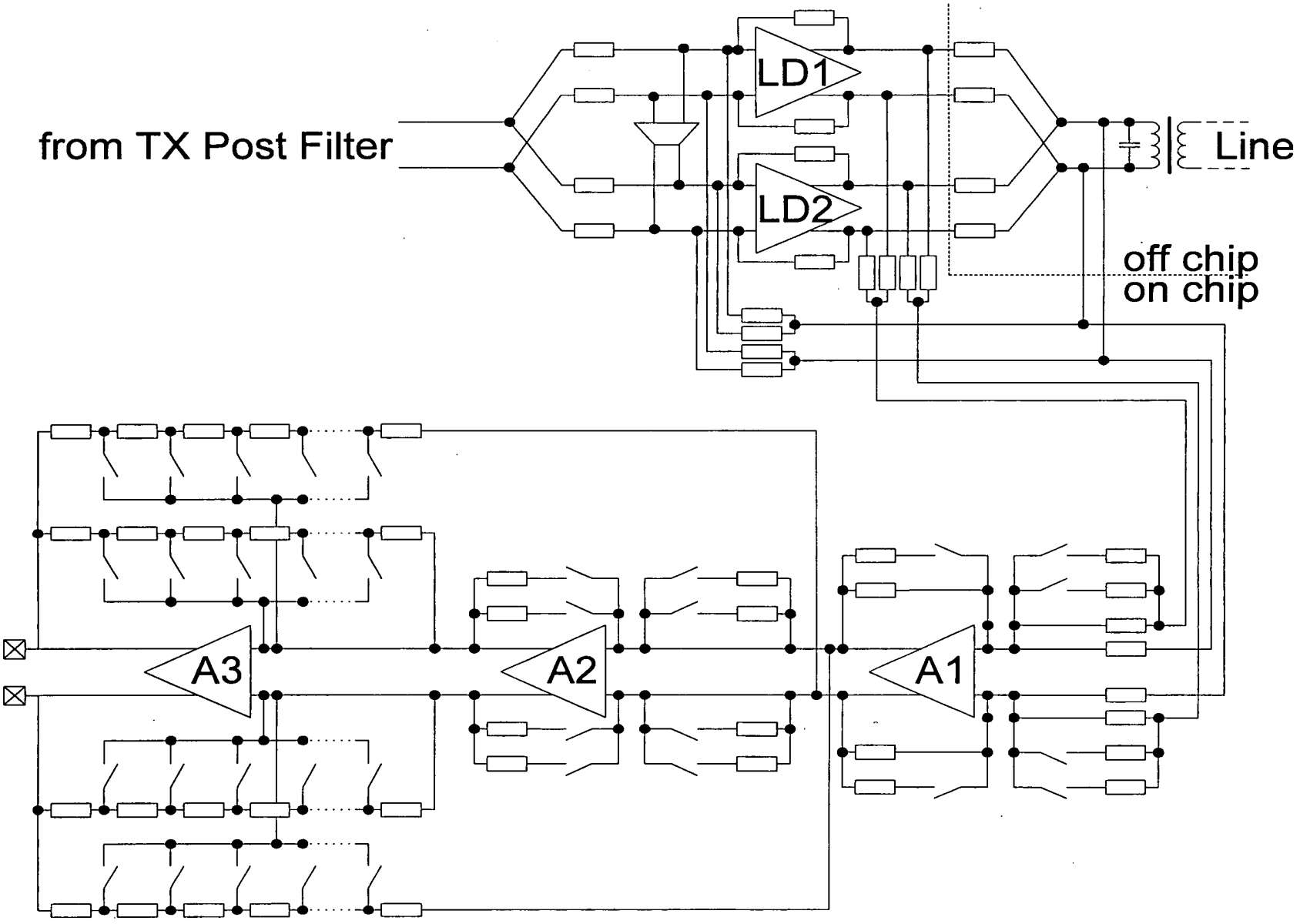

C2
C3
VDD
P2
P1
gm3
C1
gm4
C5
C4
inm
outp
outm
C6
C7
gm1
gm2
gm5
inp
N2
N1
VSS

Line Driver

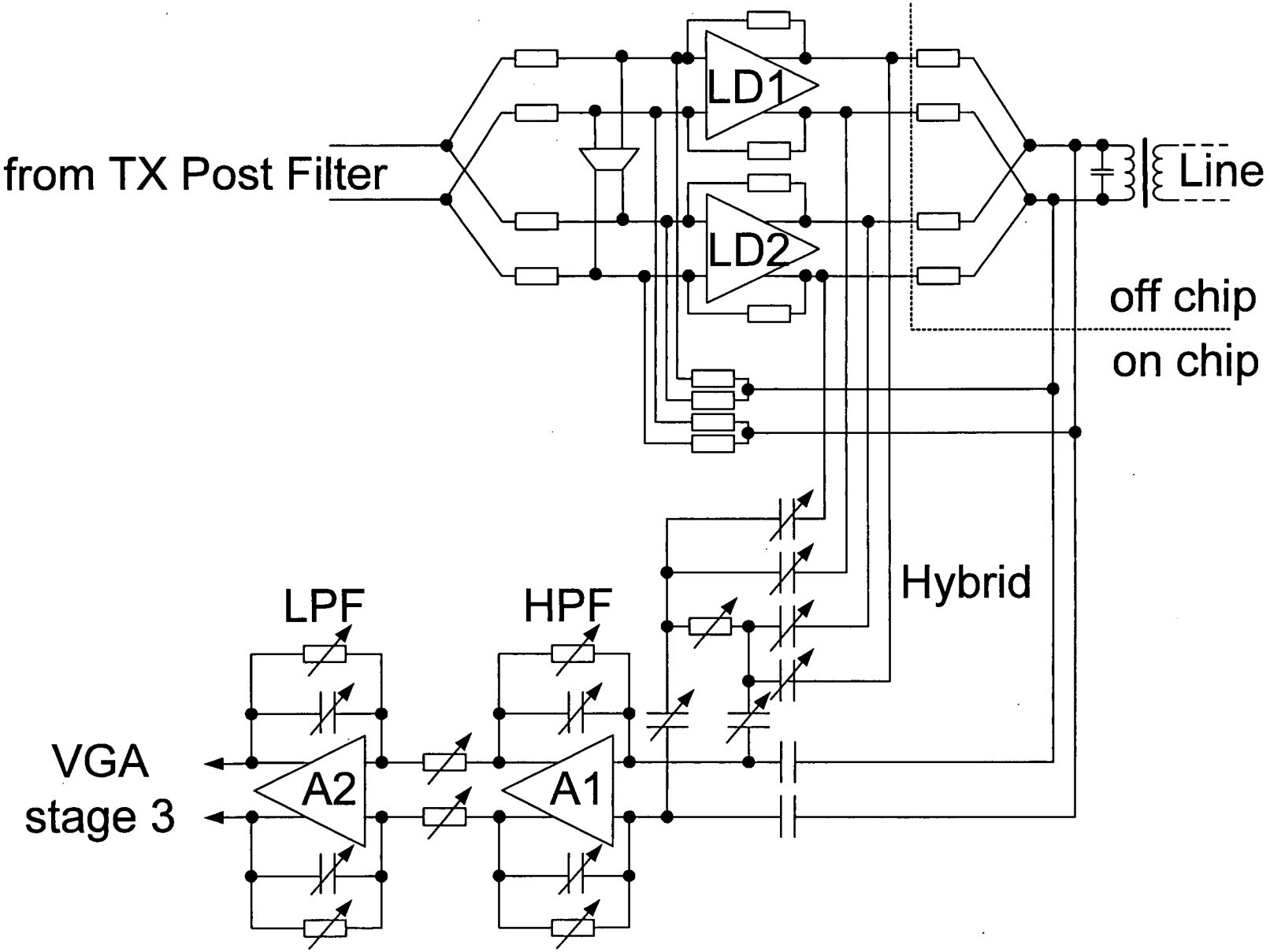


$$gm = \frac{1}{R1 \parallel R2 \parallel R3}$$

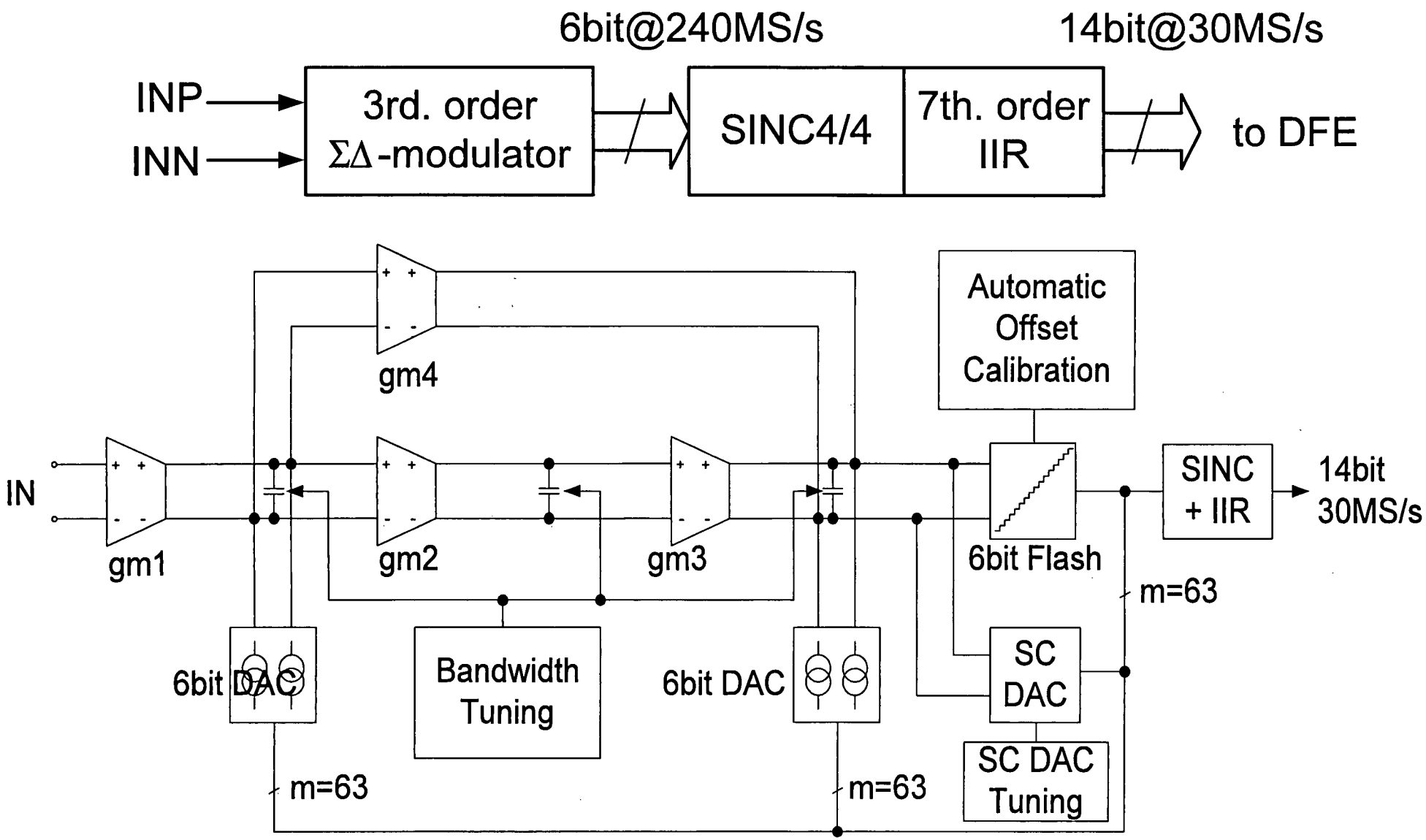
Hybrid / VGA



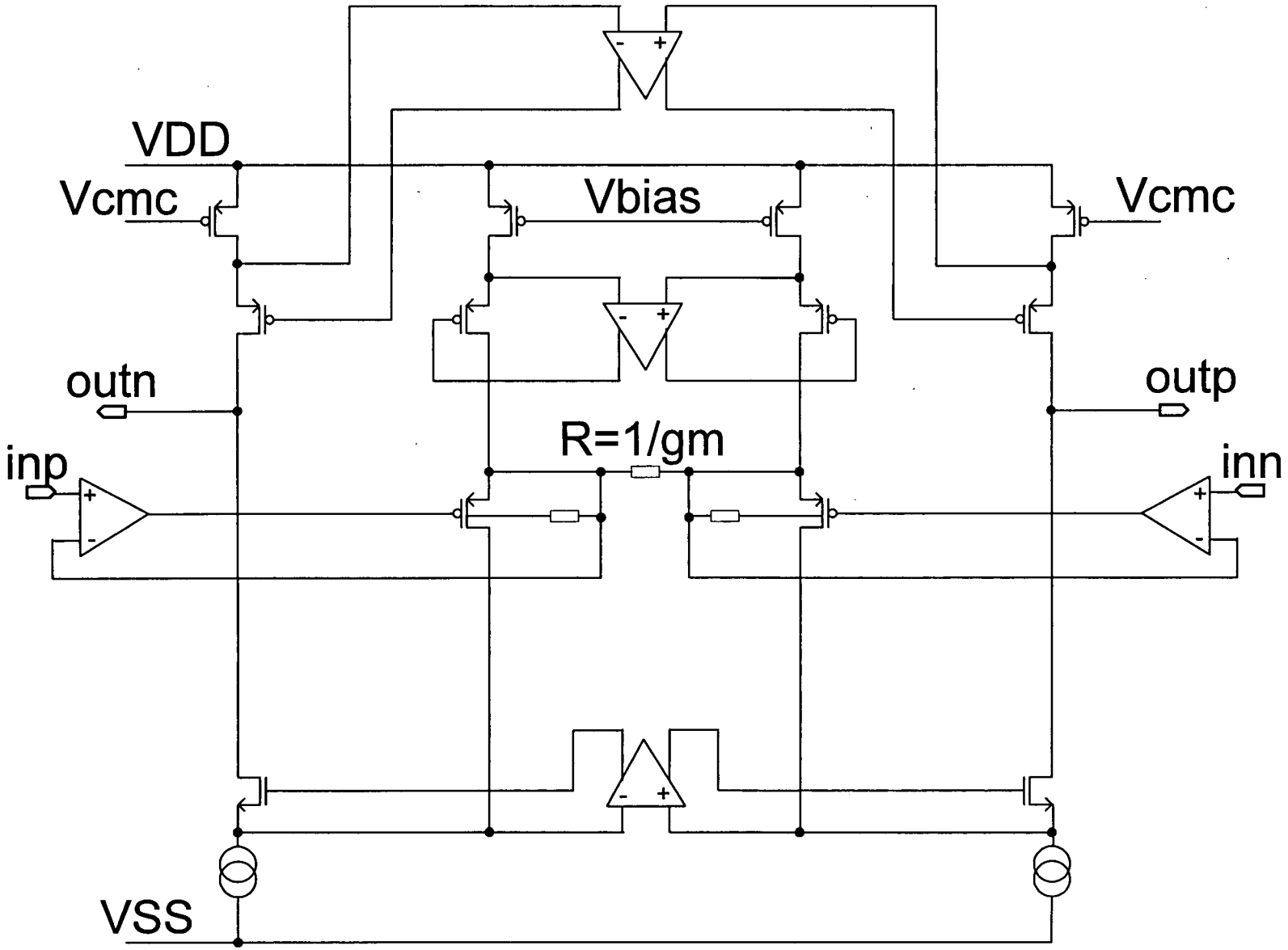
Hybrid / VGA (next revision)



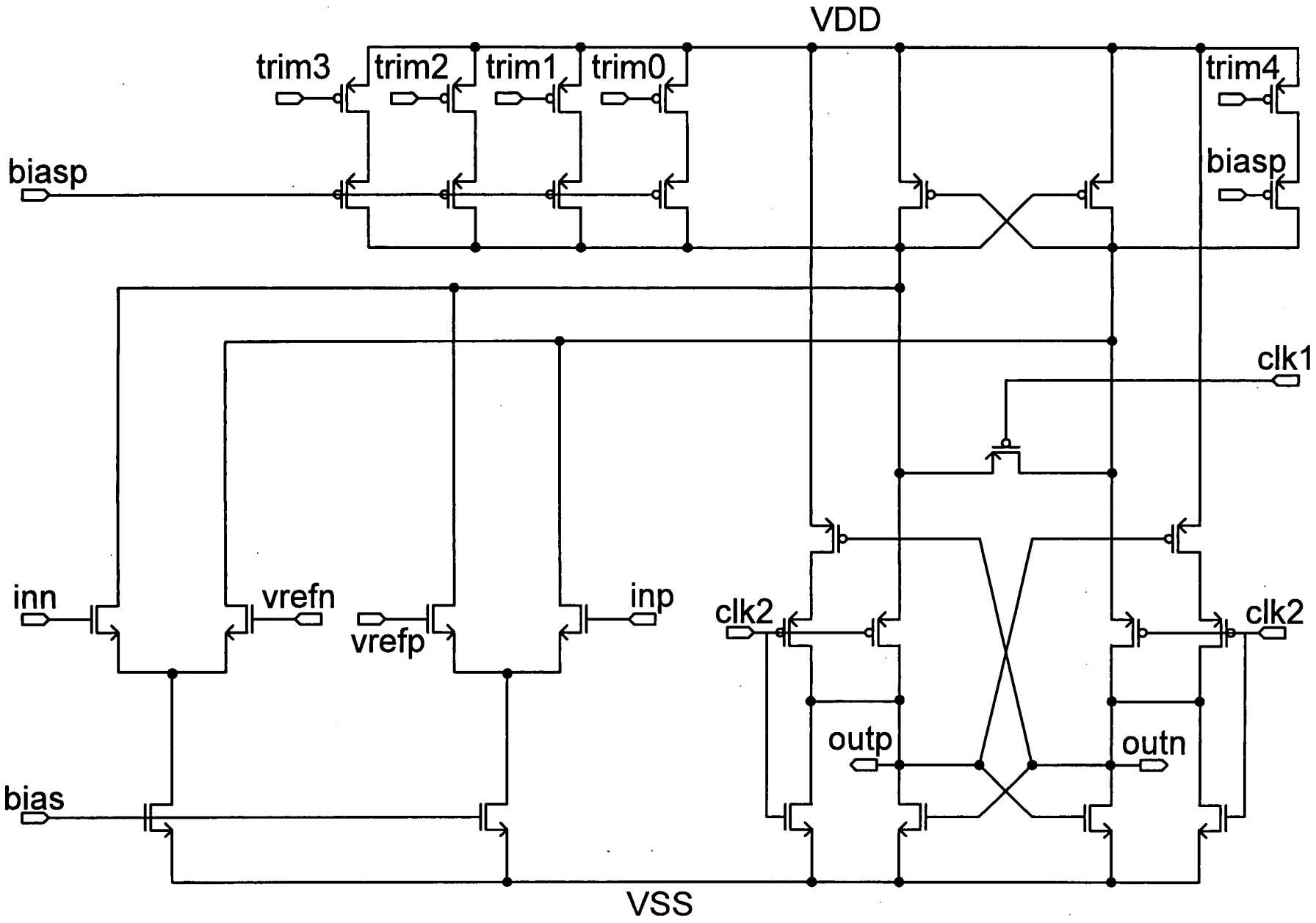
ADC


6bit@240MS/s
14bit@30MS/s
INP
INN
3rd. order
ΣΔ-modulator
SINC4/4
7th. order
IIR
to DFE
gm4
Automatic
Offset
Calibration
IN
gm1
gm2
gm3
6bit Flash
SINC
+ IIR
14bit
30MS/s
m=63
6bit DAC
Bandwidth
Tuning
6bit DAC
SC
DAC
SC DAC
Tuning
m=63
m=63

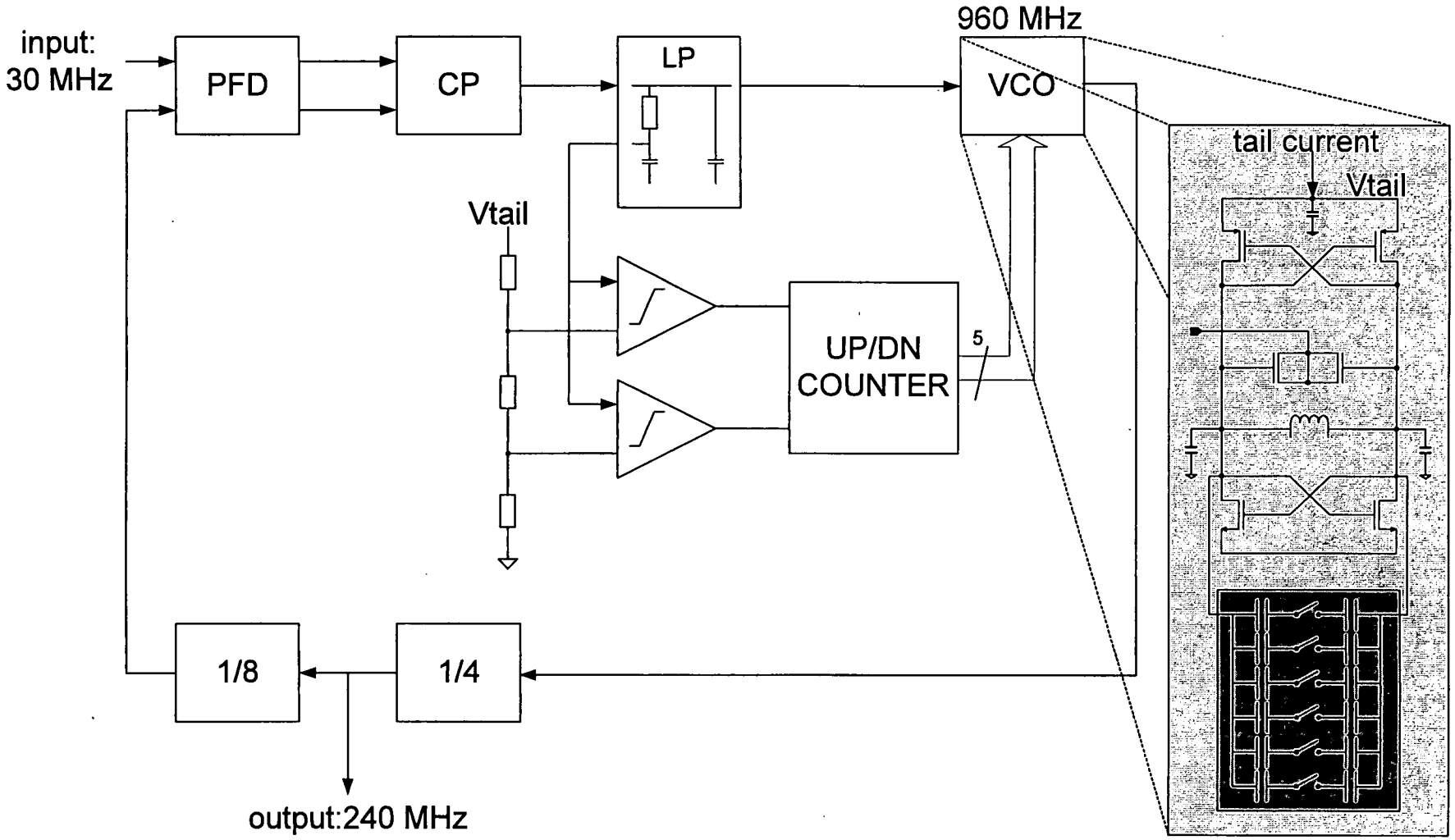
ADC GM-STAGE



ADC COMPARATOR



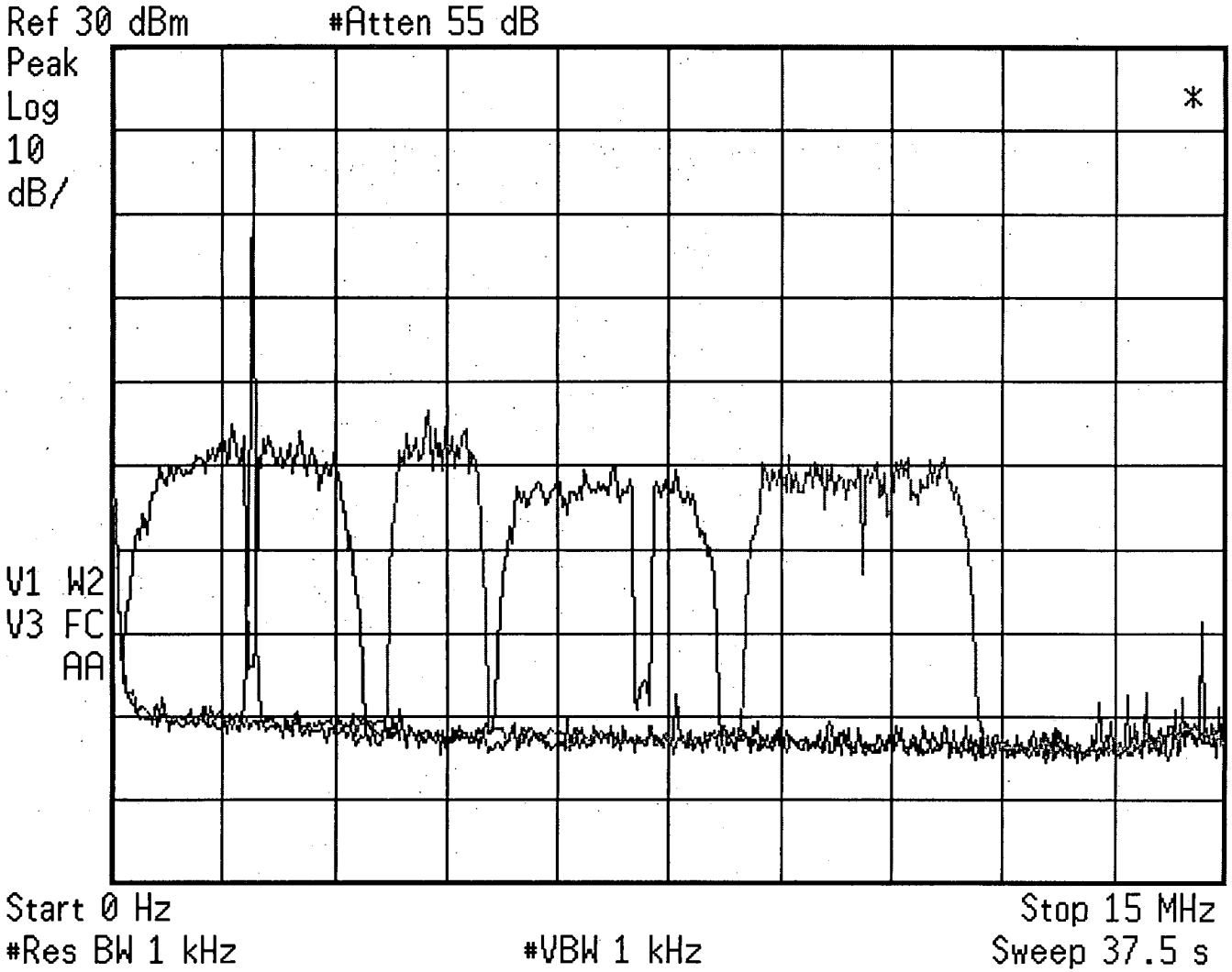
LC-PLL CIRCUIT



Measurements

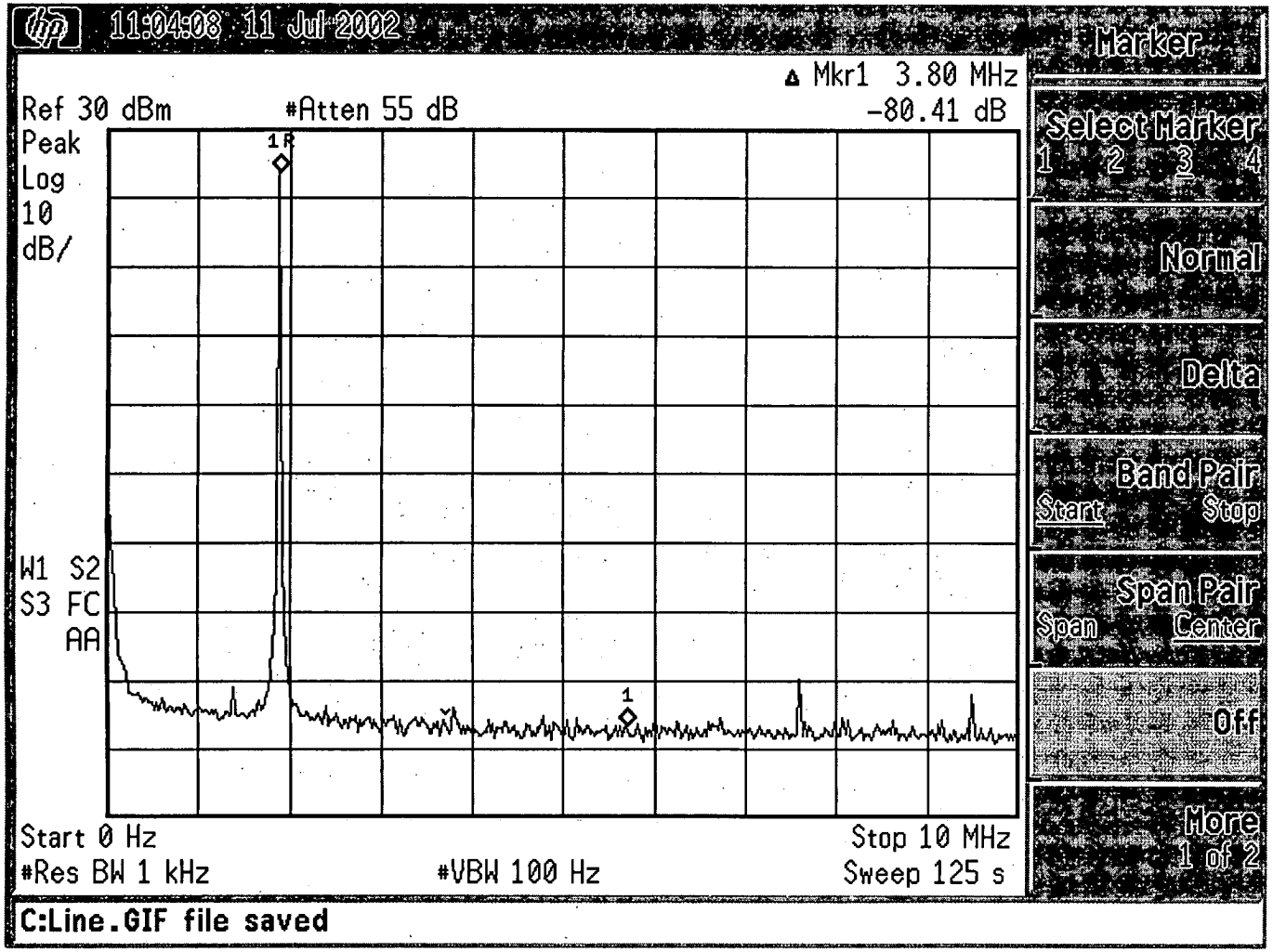
- Transmit Path and Line Driver
- Receive Path
- PLL

Transmit Path- Measurement 1



14.5 dBm signals for power measurements and functional tests

Transmit Path- Measurement 2

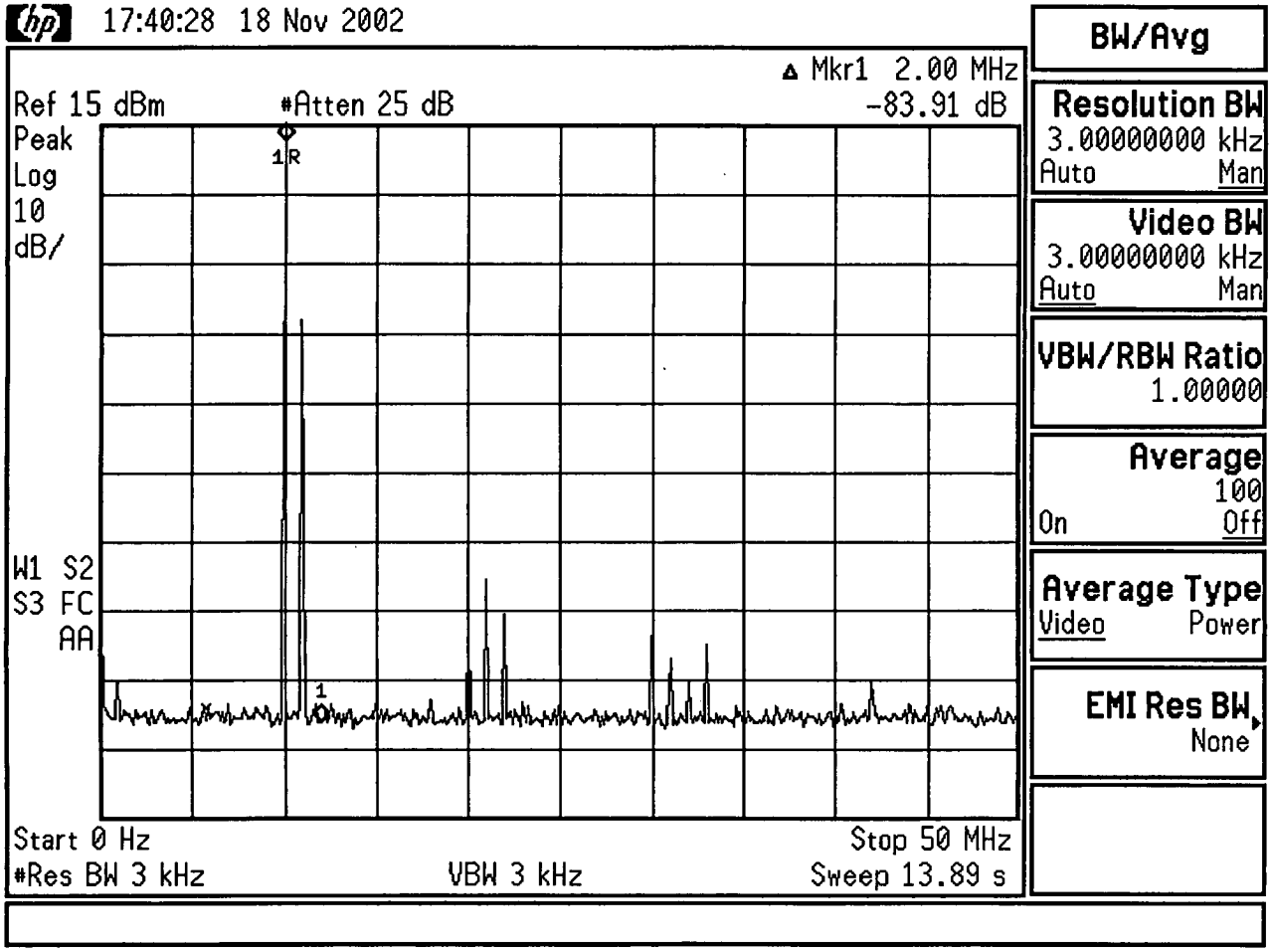


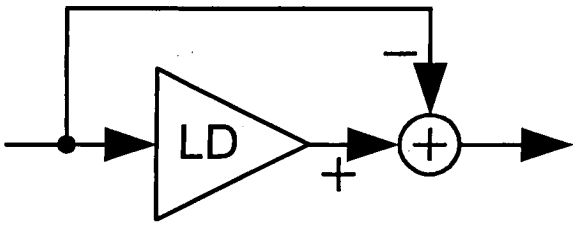
THD in 12MHz:

- 72 dBc @1.9MHz(0dBfs)

- 74 dBc @1.9MHz(- 3dBfs)

Line Driver IM3-Measurement



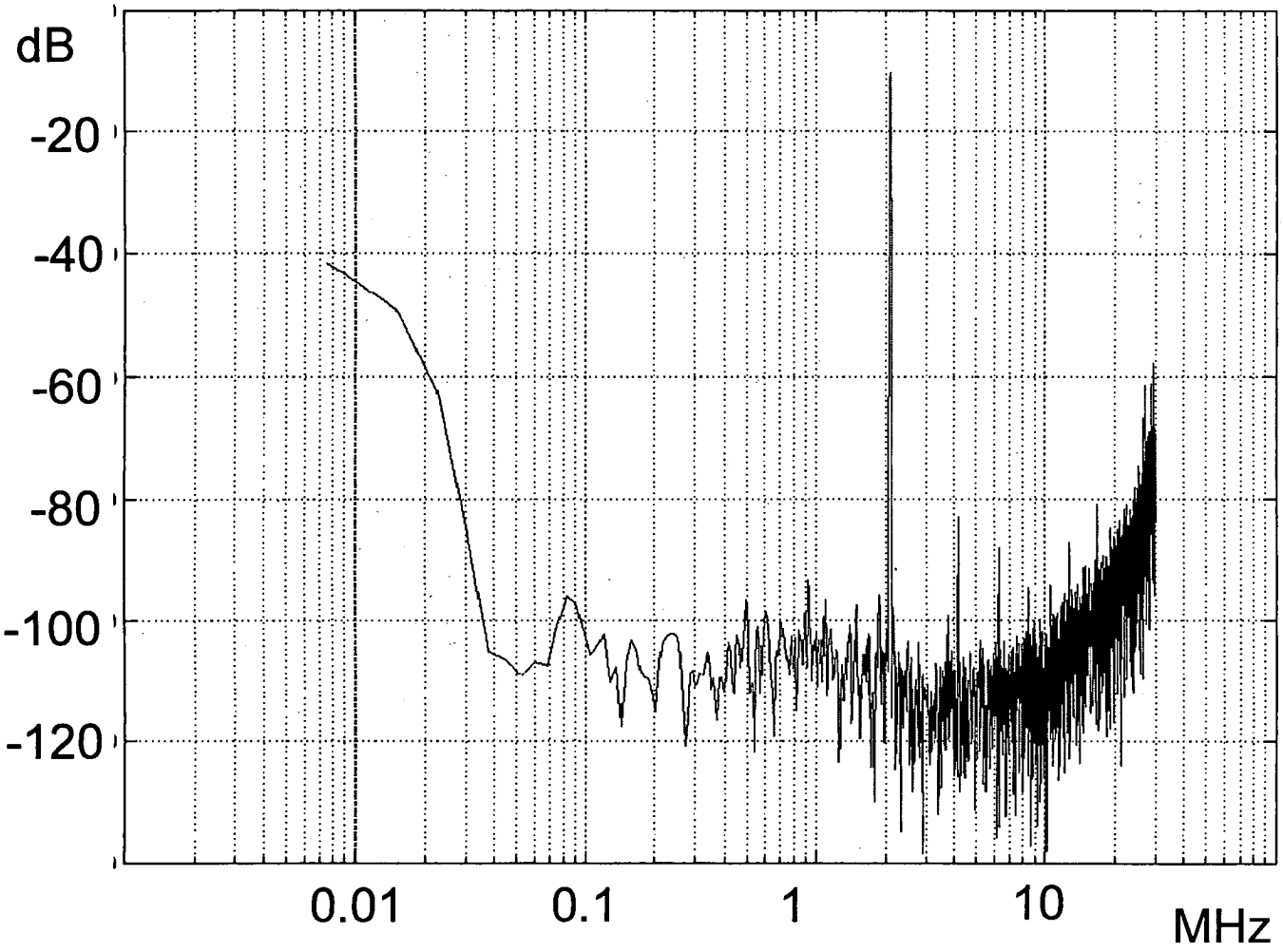


10MHz + 11MHz full scale

Input signal subtracted

IM3: below –83dBc

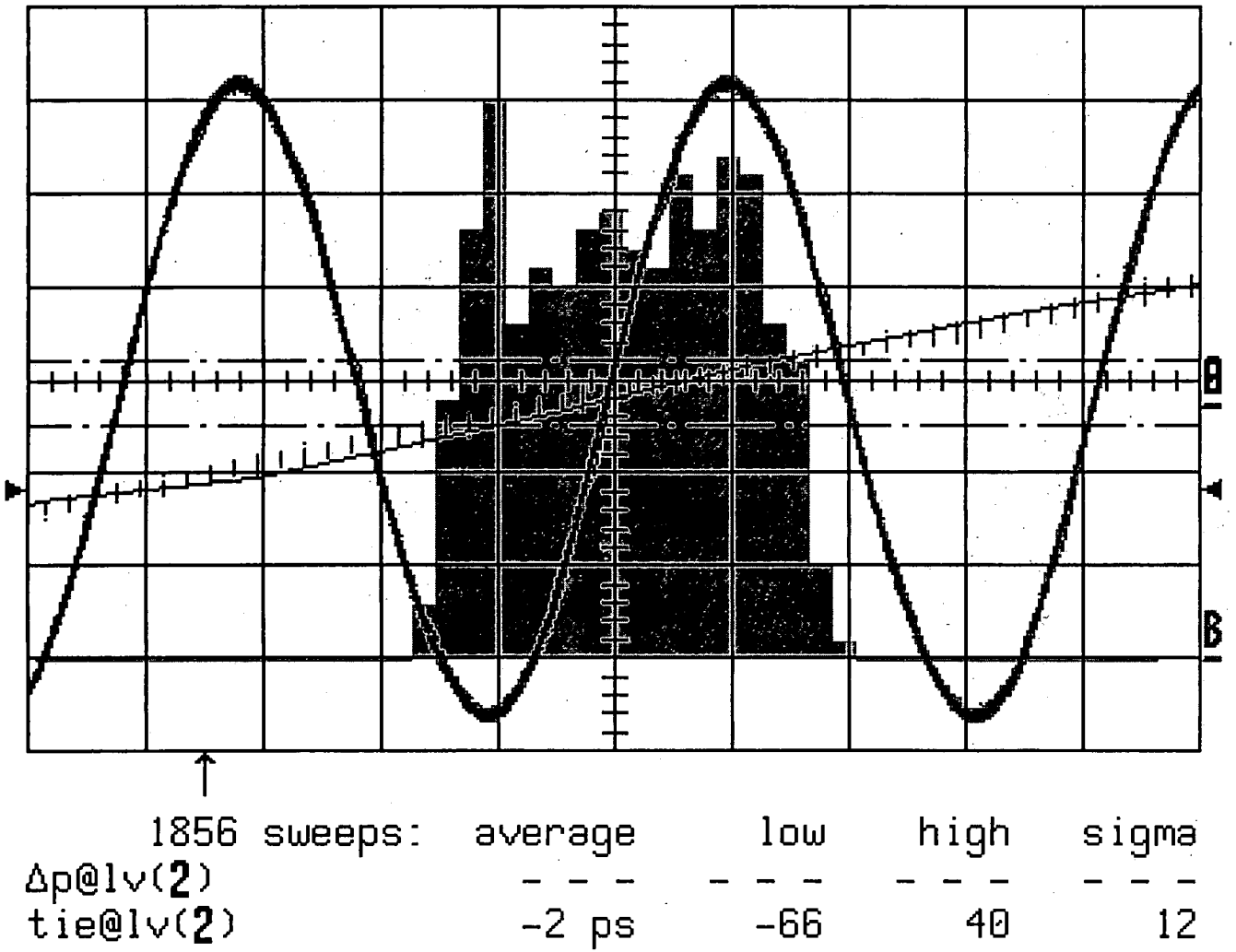
Receive Path- Measurement



2.1MHz (-1dBfs)
14 dB VGA gain

BW = 12MHz
SNR = 72dB
THD = 71dB

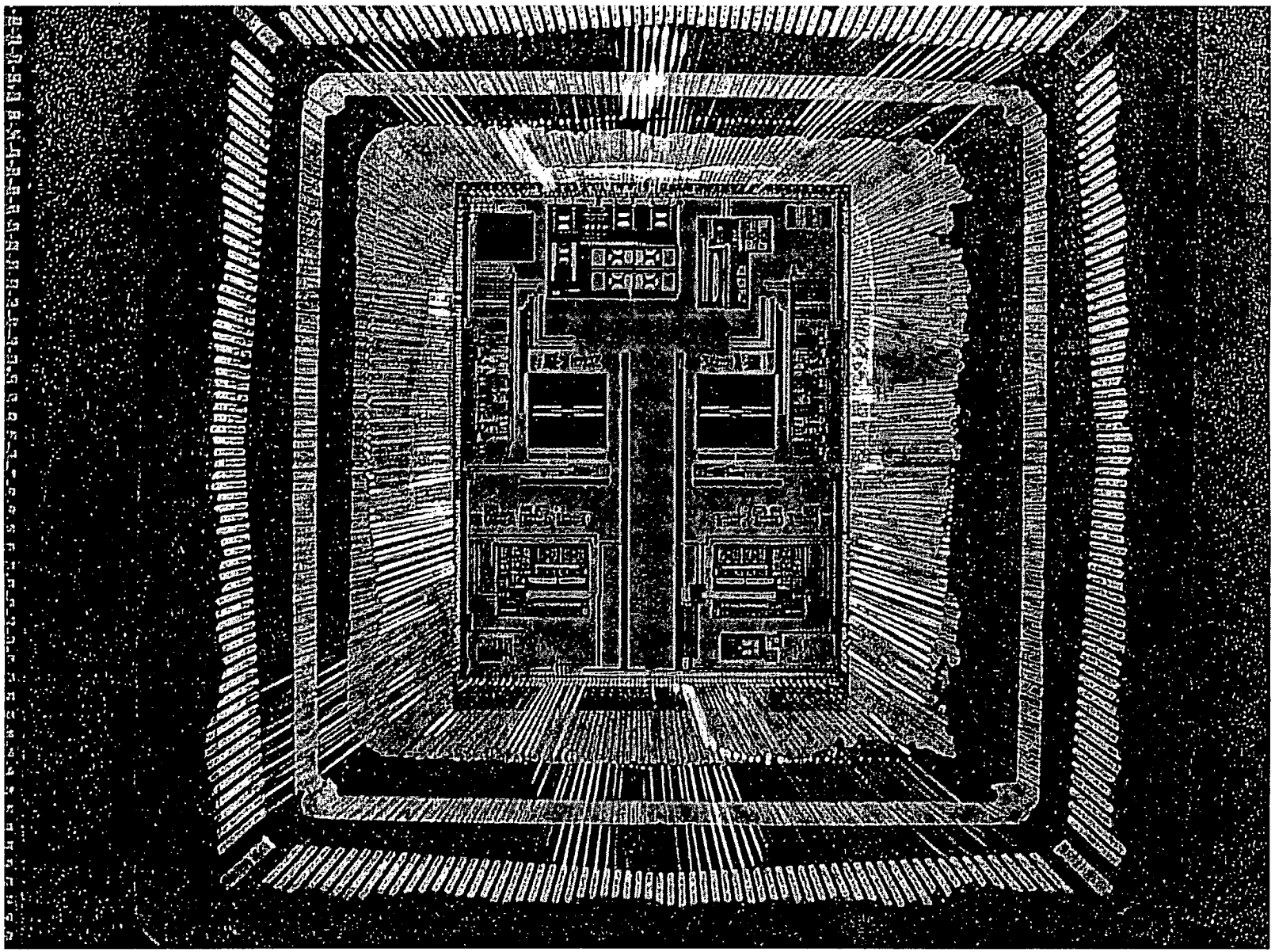
240MHz-PLL Measurement



30MHz input
240MHz output

Jitter:
12ps(rms)

Die Photo



Summary

- Dual Channel VDSL AFE
- Integrated Line Driver
- 900mW/channel power consumption at 14.5dBm line power
- 23mm²/channel (31mm² with test structures)
- 12b TX-performance at 12MHz signal bandwidth
- 12b RX-performance at 12MHz signal bandwidth

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